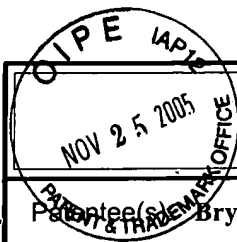


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TRANSMITTAL LETTER
(General - Patent Issued)

Docket No.
BUR920000059US1

Patentee(s) Bryant et al.

U.S. Patent No.

6,960,806 B2

Issue Date

November 1, 2005

Title: **DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Certificate of Correction
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Jack P. Friedman
Signature

Dated: 11-21-2005

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P17A/REV04

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,960,806 B2

DATED : November 1, 2005

INVENTOR(S) : Bryant et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Page 1, in the Title

Delete "DOUBLE GATED VERTICAL TRANSISTOR WITH DIFFERENT FIRST AND SECOND GATE MATERIALS" and insert --DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION--

Column 1

Lines 1-3, delete "DOUBLE GATED VERTICAL TRANSISTOR WITH DIFFERENT FIRST AND SECOND GATE MATERIALS" and insert --DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION--

Column 11

Line 53, delete "n-type" and insert --p-type--

Line 58, delete "tho" and insert --the--

Column 12

Line 9, delete "or claim 8" and insert --of claim 8--

Line 34, delete "a first safe" and insert --a first gate--

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